REMARKS

Favorable consideration of this application is respectfully requested.

Claims 1-29 are currently active in this case. Claims 24-29 have been added by way of the present amendment. Each new claim is supported by the specification and claims as originally submitted and no new matter has been added.

In the outstanding Official Action Claims 1-4, 8, 9, 13, 14, and 17-20 were rejected under 35 U.S.C. §102(e) as being anticipated by *Dupenloup* (US Patent No. 6,205,572); and Claims 5-7, 10-12, 15, 16, and 21-23 were rejected under 35 U.S.C. §103(a) over *Dupenloup* in view of *Trimberger* (U.S. Patent No. 6,084,429).

Applicants respectfully traverse the rejection of Claim 8 as being anticipated by *Dupenloup*. Claim 8 recites:

> ***8. A method for designing deep sub-micron integrated circuits, the method comprising:***
> ***performing layout of physical blocks by estimating an area for each block;***
> ***connecting pins of the blocks with no timing constraints;***
> ***assigning each wire to a metal layer pair;***
> ***optimizing the speed of each wire for its respective layer;***
> ***partitioning the blocks into cores and shells;***
> ***synthesizing the shells;***
> ***synthesizing the cores; and***
> ***recombining the shells and cores.***

However, *Dupenloup* fails to teach or suggest similar subject matter.

Applicants respectfully traverse the assertion in the outstanding Office Action which states that *Dupenloup* teach Applicants claimed *"connecting pins of the blocks (modules) with no timining constraints."* As noted in the outstanding Office Action, *Dupenloup*, at col. 70, line 63 – col. 80, line 1, discusses completing connections between proper blocks of the circuit *"disregarding the exact geometric details of each wire and terminal."* However, the exact geometric details are only delegated to the next phase (detailed routing) after an acceptable first phase (global routing) is completed (*Dupenloup*, col. 80, lines 4-8, and lines 12-16). However, although disregarding the exact geometric details of each wire and terminal may have an effect on timing constraints, the geometric details of a wire are not dispositive of timing constraints. More importantly, geometric details disregarded in *Dupenloup* refers to items such as the wire width, and layer assignment, which are not a specification or teaching for disregarding all timing constraints. In contrast, the claimed invention requires that the pins be connected without timing constraints.

Applicants respectfully traverse any assertion in the outstanding Office Action that would indicate or imply *Dupenloup* teaches *"optimizing the speed of each wire for its respective layer."* However, *Dupenloup* only resolves timing issues related to specific timing violations encountered, and does not *optimize speed* for *each wire*. More specifically, the cited section at col. 41, lines 11-28 describes a typical determination of a timing violation (e.g., lines 19-20 *"it would be possible to have a timing violation...,"* and line 21 *"Another problem is illustrated ...,"* and lines 23-24 *"Finally, another problem illustrated by the figure ..."*). Col. 41, line 28 – col. 42 line 40 go on then to describe further mapping, simulations and clock allocations to resolve timing problems. Finally, at col. 42, lines 41-47, *Dupenloup* succinctly describes how that many timing iterations will likely be needed before all timing violations can be fixed. In contrast, the claimed invention optimizes the speed of each wire. While optimization of wires may be done at the expense of chip real estate, the expense minimizes or eliminates the

"very difficult and time consuming task" of time budgeting and iterations to solve the then occurring timing violations in the more traditional manners like that described in *Dupenloup* (*Dupenloup*, col. 42, lines 41-45 which describes and admits the very problem Applicants invention avoids, compare to Applicants specification, page 18, lines 14-17).

The other cited portions of *Dupenloup* also indicate that *Dupenloup* is not describing Applicant's claimed method. For example, at col. 70, lines 45-52, *Dupenloup* describes how timing constraints are utilized (timing constraints evolve throughout synthesis), and are eventually met (*"meeting timing constraints"*). And, Col. 80, lines 12-17 only show that *Dupenloup* utilizes two routing phases (global and detailed), which does not lend support to optimal speed in each wire as claimed. Therefore, Applicants respectfully submit that the claimed invention cannot be anticipated by *Dupenloup* because *Dupenloup* fails to teach or suggest subject matter specifically claimed in Claim 8. Accordingly, Applicants respectfully submit that Claim 8 is patentable over *Dupenloup*.

Applicants respectfully traverse the rejection of Claim 13 as being anticipated by *Dupenloup*. Claim 13 recites:

> ***13. A method for reducing design cycle time for integrated circuits, the method comprising:***
> ***laying out blocks by estimating an area for each block;***
> ***minimizing a delay in each global wire;***
> ***partitioning each block into a core and a shell;***
> ***performing logic synthesis an each shell by utilizing a known delay for each wire;***
> ***performing logic synthesis on each core; and***
> ***recombining the shells and cores.***

However, *Dupenloup* fails to teach or suggest similar subject matter.

Applicants specifically traverse any assertion that indicates *Dupenloup* as teaching Applicants claimed *"minimizing a delay in each global wire."* As noted above, the cited portions of *Dupenloup* discuss timing violations, meeting of timing constraints, and performing routing in global and detailed routing phases. However, none of that indicates minimizing delay in each global wire. Further, *Dupenloup's* described processes are instead mainly aimed at minimizing area (saving space), meeting timing constraints, or minimizing gate counts (*Dupenloup*, col. 70, lines 50-52) consistent with contemporary design methods, but the present invention sacrifices chip real estate to reduce design cycle time by maximizing wire performance and eliminating multiple iterations of adjusting timing to fit minimally sized designs. Therefore, Applicants respectfully submit that Claim 13 cannot be anticipated by *Dupenloup* because *Dupenloup* fails to teach or suggest a similar design strategy and fails to teach or suggest subject matter specifically claimed in Claim 13. Accordingly, Applicants respectfully submit that Claim 13 is patentable over *Dupenloup*.

Applicants respectfully traverse the rejection of Claim 1 under 35 USC 102(e) as being anticipated by *Dupenloup*. Claim 1 recites:

> ***1. A method for synthesizing an integrated circuit design, the method comprising:***
> ***performing physical optimization of block and wire placement, before performing logic synthesis;***
> ***partitioning the blocks into cores and shells;***
> ***synthesizing the shells and cores; and***
> ***recombining the cores and shells into blocks.***

However, *Dupenloup* fails to teach or suggest the same subject matter.

Applicants respectfully traverse the assertion in the outstanding Office Action that equates discussion in *Dupenloup* (e.g., at col. 10, lines 8-22, and col.

15, lines 20-47), regarding modules/sub-modules and combinational logic/output being registered or driven by a flip-flop, as being comparable or teaching Applicants' claimed *"partitioning the blocks into cores and shells."*

Applicants admit that *Dupenloup* discusses partitioning of a design into modules of lower complexity (*Dupenloup*, col. 10, Line 9). However, modules or blocks are generally known to be portions of circuits containing a set of discrete inputs, outputs, and related logic. Sub-modules are generally known to be blocks within a module (or blocks within blocks), that are generally utilized to break the design into more fundamental components. In contrast, shells and cores are portions of a block that not only break a design into components, but also meet specific definitional requirements. Primarily, those definitional requirements, as elaborated on in Applicants' specification, define a core as the logic in a block bounded by registers, and a shell as the logic between a core and the pins of the block (e.g., see Applicants' specification page 8, lines 16-18). However, *Dupenloup* gives no consideration to shells and cores as defined by Applicants.

Therefore, even if Applicants' claimed shells and cores are somehow construed as sub-blocks, *Dupenloup* still fails to teach or suggest Applicants' claimed invention because the blocks and sub-blocks of *Dupenloup* only define a broad categorization that generically describes any hierarchical breakdown of a circuit into its component groups. *Dupenloup* fails to describe blocks and/or sub-blocks that meet Applicants' shell and core definition (Claim 1 requires the partitions be made via shells and cores, not simply the broader blocks and/or sub-blocks, or sub-blocks that are pure or logic only circuits as described in *Dupenloup*).

Applicants respectfully traverse any assertion that would equate registration of outputs (driven by flip-flops, col. 15, ll. 37-47) to any part of Applicants' *"partitioning the blocks into shells and cores."* Primarily, the registration of

outputs or use of flip flops to drive outputs (and/or any separate compilation of modules having registered outputs) is not the same as partitioning a block into cores and shells.

Applicants also respectfully traverse any assertion that would equate *Dupenloup's* further statements regarding extraction of logic that surrounds memories (col. 15, ll. 58-60) as teaching any part of Applicants' claimed invention. In particular, Applicants respectfully note that, as defined in Applicants' specification, shell and core partitioning is performed on logic between memory elements and logic before or after a memory element in a block. However, extracting logic that surrounds a memory only teaches or suggests an extraction of the logic, but extracting logic does not teach or suggest a partitioning of the block into cores and shells – they are completely different operations.

Therefore, Applicants respectfully submit that Claim 1 cannot be anticipated by *Dupenloup* because *Dupenloup* fails to teach or suggest subject matter specifically claimed in Claim 1. Accordingly, Applicants respectfully submit that Claim 1 is patentable over *Dupenloup.*

Applicants further respectfully traverse the rejection of Claim 5 as being anticipated by *Dupenloup*, and/or obvious over a combination of *Dupenloup* and *Trimberger.* Claim 5 recites:

> ***5. (Original) The method of Claim 4, wherein performing physical optimization of wire placement further comprises minimizing a delay in each wire by inserting buffers at optimal distances.***

However, neither *Dupenloup* nor a combination of *Dupenloup* and *Trimberger* teach or suggest similar subject matter.

As noted above, *Dupenloup* fails to teach minimizing delay or maximizing performance in each wire. At best, *Dupenloup* teaches iterations to meet timing constraints. However, the iterative process for meeting timing constraints is precisely one of the main motivating premises for the invention as claimed in Claim 5, which is to eliminate those iterations. More importantly, Claim 5 specifically recites minimizing delay in each wire which is neither taught nor suggested by *Dupenloup*. Therefore, Applicants respectfully submit that Claim 5 cannot be taught or suggested by a combination of *Trimberger and Dupenloup* because neither reference teaches or suggests subject matter specifically claimed in Claim 5.

Applicants respectfully traverse any assertion that indicates *Timberger* teach minimizing delay in each wire by inserting optimally spaced buffers. As a preliminary matter, Applicants respectfully note that *Trimberger* relates to an improvement in programmable logic devices and is not synthesizing an integrated circuit design as claimed in Claim 5. Therefore, Applicants respectfully traverse any combination with *Trimberger* because *Trimberger* is not related enough to either *Dupenloup* or the claimed invention so as to form a proper combination.

Nevertheless, and more importantly, Applicants respectfully note that *Trimberger* teaches segmented and staggered routing to reduce loading in a programmable logic device so that buffers can be removed (e.g., *Trimberger*, col. 2, lines 3-6). However, removing buffers teaches away from the subject matter claimed in Claim 5 which recites inserting buffers. Moreover the reason buffers are inserted by the claimed invention is entirely different from the reason *Trimberger's* buffers are removed (*Trimberger* removes buffers because they are no longer needed to support loading, and Claim 5, unconcerned with loading, adds buffers to make the wires as fast as possible). Therefore,

Applicants respectfully submit that *Trimberger* does not teach any part of Applicants claimed invention. Accordingly, Applicants respectfully submit that Claim 5 is patentable over *Dupenloup* and *Trimberger*.

Applicants respectfully submit new Claims 24-39. Each new claim is either dependent upon a claim already believed to be patentable or includes subject matter related to minimizing delay in each global wire as neither taught nor suggested by *Dupenloup*. Further subject matter present in each claim provides yet further patentable distinctions over the cited art.

Based on the patentability of independent Claims 1, 8, 13, and 24, and the further discussion with respect to dependent Claim 5, Applicants further respectfully submit that dependent claims 2-7, 9-12, 14-22, 25-29 are also patentable.

If the Examiner disagrees with any of the foregoing, the Examiner is invited to telephone the undersigned who will be happy to work with the Examiner in a joint effort to derive mutually satisfactory claim language.

Consequently, no further issues are believed to be outstanding, and it is respectfully submitted that this case is in condition for allowance. An early and favorable action is respectfully requested.

Respectfully submitted,
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Dated: 04 Aug '05

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